Exhibit A
to the
Declaration of Sabin Head In Support of Visto's Motion for Preliminary Injunction

Exhibit A

Curriculum Vitae

Sabin R. Head, Ph.D.

EDUCATION

B.A. (Honors) Psychophysics, Harvard College 1965.
(Minors in Math and Physics. Dissertation on sensory midlines.)

Ph.D. Sensory Intelligence, The University of Michigan, 1972/74.
(Electrical Engineering and Experimental Psychology Departments. Dissertation on Acoustic Imaging, Small Signal Analysis, Mathematically Ideal and Quasi-Ideal Observers)

SUMMARY OF INDUSTRIAL EXPERIENCE

1987 – Present: Independent Consulting

Independent consultant to the high-technology community. Dr. Head has consulted on numerous projects including computer hardware and software, semiconductor design tools, computer-integrated manufacturing, software code analysis, operating system and network operating system analysis, distributed and clustered computing systems analysis, data compression, large scale robotic mass storage systems, CAD/CAM/CAE, video games, databases, search engines, video compression, including areas of patent and copyright analysis, trade secrets, and product fitness.

3/87-7/88 - Systems Architect, Calma Corporation (subsidiary of General Electric, later acquired by Valid Logic). Chief architectural position for commercial logic design tools. Responsibilities included redesigning and replacing the previous obsolete line of logic design tools; defining new logic tools for an integrated logic and layout design environment. Also responsible for finding, evaluating, and negotiating with appropriate OEM parties for existing tools.

1/86-2/87 – Principal Investigator, Wright Patterson Air Force Base (SBIR contract). The purpose of this fixed-term Small Business Innovative Research contract was to develop an advanced Entity-Relation (ER) modeling paradigm for multi-processor design for the 1990s. The business strategy, risk assessment, and manufacturing components were integrated with the design component itself. As sole investigator on the project, he authored the proposal, designed a Prolog-like modeling language on which the rest of the system was based, developed a hybrid modeling paradigm incorporating both Entity-Relation and Petri Net formalisms, programmed the prototype simulator that was the system's "proof of concept" and co-authored the final report with the president of the SBIR contracting firm Patsi (Palo Alto, CA).

11/84-12/85 – System Architect, Tangent Corporation (start-up, now part of Cadence). Chief architectural position responsible for system-wide architectural issues for a commercial Standard Cell computer chip layout system, with a special focus on database design issues and open-system interfaces. Also developed a formal Petri Net environment manager for human-computer chip design dialog; provided for tracking, enforcement and display of design process interdependencies; provided for design backtracking and incremental re-design; designed a novel quasi-relational database for engineering data.

8/83-11/84 – CAD Manager, Zilog Corporation (subsidiary of Exxon, turnaround effort). Primary mission was schedule recovery on several major VLSI chips by integrating and improving the designers' CAD/CAM/CAE environment. Managed the internal simulator project, increasing its speed, power, and scope; introduced fault simulation to detect design errors and untestable circuitry; corrected existing non-operational verification tools; achieved first-silicon results for the Zilog Z80,000 32-bit microprocessor. Managed the electrical engineering department's Digital VAX Cluster distributed computer system and assisted purchase and installation of its MVS-based Amdahl mainframe.

7/82-8/83 – Logic and Simulation Design Manager, CAE Systems (startup, later part of Tektronix). Chief architectural position responsible for electronic logic system description languages and simulation interfaces for a commercial automated layout system.

2/78-7/82 – Lead CAD Developer, Data General Corporation, Semiconductor Division. Division's first full-time CAD developer as it moved from 16-bit to 32-bit microprocessors. Wrote novel multilevel logic simulator using recursive descent scheduling, wrote control-path description language for logic synthesis and optimization. Chaired corporation's nation-wide simulation committee, was part-time acting CAD manager.

1972-1977 – Research Faculty, The University of Michigan. This position was equivalent to an Associate Professor but was non-voting. Director of Research Evaluation for 125-person contract research facility; supervised all projects and proposals with respect to research methodology. Principal Investigator in a multi-year $1.2 million research survey project; supervised, edited, and produced a four-volume research review series; planned and designed a series of national research dissemination workshops; ran the workshops for three years with faculty from 250 universities participating annually. Taught undergraduate research methodology, supervised six graduate students per year.

PRESENTATIONS AND PUBLICATIONS

Procedural Entity-Relation Modeling for the Enterprise of Multiprocessor Digital Systems Design", Sabin Head & Patricia Weiner, Final Report, Wright-Patterson Air Force Base Project No. F33615-86-C-1109 (1987).

"Petri Nets for Interactive Design Process Control, with Rip-Up and Backtracking", proprietary, Tangent (1985).

"Architectural Specification for a Quasi-Relational Data Base for both Design Data and Multiple-Foundry Libraries of Standard Cells", proprietary, Tangent (1985).

"Zycad Implementation of ASIM Simulation: Design and Benefits", proprietary, Zilog (1984).

Chairman, session "Design Automation and Artificial Intelligence", speakers Narinder Singh (Stanford & Fairchild), Prof. Larry Wos (Univ. Ill. & Argonne Labs), Dr. Ed Cheng (Silicon Compilers Inc.), Walling Cyre (CDC). IEEE Design Automation Workshop, Lansing, MI (1984).

Chairman, session "Engineering Workstations and Designer Productivity", speakers Rob Rutenbar (Univ. Mich.), Hin Kim (Carnegie Mellon), Narinder Singh (Stanford & Fairchild), Don Schuler (Prime). IEEE Design Automation Workshop, Lansing, MI (1983).

"CALC: a Frames-Based Designer's Calculator Interface to the Design Data Base, with Embedded LISP", proprietary, CAE Systems (1983).

Chairman, session "Logic Design Automation", speakers Prof. Mike Genesereth (Stanford), Dr. Harold Brown (Stanford), Dr. Howie Schrobe (Symbolics), Chris Terman (MIT & Symbolics), Michael Heydemann (U. Colorado), David Allenbaugh (Zycad). IEEE Design Automation Workshop, Lansing, MI (1982).

"CDL: Design and Specification of a Control Path Description Language and its Synthesis of Tegas Code", proprietary, Data General (1982).

"PSIM: Simple Recursive Descent Scheduling in Behavioral Simulation", proprietary, Data General (1982).

Chairman, National Corporate Simulation Committee, Data General (1982).

"Switch Simulation in the Context of Tegas, a Traditional Logic Simulator", IEEE Design Automation Workshop, Lansing, MI (1981).

TESTIMONIAL EXPERIENCE

Zilog v. Zycad, c. 1986, Wisconsin. Deposed as Percipient Witness. Issue: hardware logic simulation engine, fitness for purpose.

Data General v. Grumman, c. 1991, Federal Court, Boston, Massachusetts. Testified as Expert Witness on Grumman's behalf. Issue: trade secrets, copyright infringement.

Microsoft v. Stac, c. 1995, Federal Court, Los Angeles, California. Testified as Expert Witness on Microsoft's behalf. Issue: trade secrets (countersuit).

Bell Atlantic v. STK, c. 1996, San Francisco, California. Deposed as Expert Witness on behalf of Bell Atlantic, which became Decision One during the proceedings; case settled. Issue: copyright, trade secrets.

Novell v. Timpanogas Research Group, 1997, Provo, Utah. Testified as Expert Witness on TRG's behalf. Issue: theft of trade secrets by departing employees, temporary restraining order hearing.

Bellcore v. Unisys, 1997, Somerset, New Jersey. Deposed as Expert Witness, attended binding arbitration hearing but was not called to testify. Issue: contract default.

CRT v. Ameritech, 2000, Detroit. Deposed as Expert Witness on behalf of CRT, case settled. Issue: trade secrets.

Bar None v. Duncan Group, 2001, San Jose, California. Deposed as Expert Witness on behalf of Bar None, case settled. Issue: contract default.

IKOS & MIT v. AXIS, San Jose, California (2001-ongoing). Expert Witness on behalf of AXIS. Issue: software & hardware patents. IKOS has been purchased by Synopsis during the proceedings.

LRS v. PACE, Federal Court, Golden, Colorado (2000-2002). Testified as Expert Witness on behalf of PACE. Issues: trade secrets, fraudulent misrepresentation, duty of loyalty.

Apple Computer v. Sorenson, Federal Court, San Jose, California (2002). Expert witness on behalf of Sorenson. Issues: trade secrets, software patents, breach of contract.

Library Technologies, Inc. v. Virtual Silicon, Inc., Arbitration, Palo Alto, California (2003). Testified on behalf of Library Technologies. Issues: copyright, trade secrets, breach of contract.

CCITriad v. Car Parts Inc., Texas (2003). Expert witness on behalf of CCITriad. Issues: Copyright, trade secrets. Deposed, case settled.